AMENDMENTS TO THE CLAIMS

Upon entry of the present amendment, the status of the claims will be as shown below. This listing of claims replaces all previous versions and listings of the claims in the present application.

Listing of Claims

1. (Currently Amended) A cache memory, comprising:

an addition unit ~~operable to add~~ which adds, to each cache entry holding line data, a caching termination attribute indicating whether or not caching of the cache entry is allowed to be terminated;

a selection unit ~~operable to select~~ which selects a cache entry that has been added with a caching termination attribute indicating that caching is allowed to be terminated, and has been set with a dirty flag indicating that the cache entry has been written into; and

a write back unit ~~operable to write back~~ which writes back, to a memory, line data of the selected cache entry, regardless of an occurrence of a cache miss,

a holding unit which holds an address range specified by a processor, said holding unit being configured as a register that can be accessed by the processor through an instruction;

a search unit which searches for a cache entry holding line data within the address range held in said holding unit; and

a setting unit which sets, to the searched-out cache entry, the caching termination attribute indicating that caching is allowed to be terminated, while said cache memory is not being accessed by the processor;

wherein storing of the address range in said holding unit is performed according to a data transfer instruction for transferring data to said holding unit.

2. (Canceled)

3. (Currently Amended) The cache memory according to Claim [[2]] 1,

wherein said search unit includes:

a first conversion unit ~~operable~~ which, in the case where a start address of the address range held in said holding unit indicates a point midway through line data, ~~to convert~~ converts the start address into a start line address indicating a start line included in the address range;

a second conversion unit ~~operable~~ which, in the case where an end address of the address range held in said holding unit indicates a point midway through line data, ~~to convert~~ converts the end address into an end line address indicating an end line included in the address range; and

a judgment unit ~~operable to judge~~ which judges whether or not there exist cache entries holding data corresponding to respective line addresses from the start line address to the end line address.

4. (Currently Amended) The cache memory according to Claim [[2]] 1, further comprising:

a replacement unit ~~operable~~ which, when a cache miss occurs, ~~to select~~ selects, as a subject for replacement, the cache entry that has been added with the caching termination attribute indicating that caching is allowed to be terminated.

5. (Currently Amended) The cache memory according to Claim 1,

wherein said addition unit includes:

an instruction detection unit ~~operable to detect~~ which detects execution, by a processor, of a store instruction having, as instruction details, addition of the caching termination attribute indicating that caching is allowed to be terminated, and writing of data; and

a setting unit ~~operable to set~~ which sets the caching termination attribute to a cache entry that has been written into in accordance with the detected instruction.

6. (Currently Amended) The cache memory according to Claim 1,

wherein said write back unit ~~is operable to write back~~ writes back data of a cache entry to the memory, when a memory bus has an idle cycle.

7. (Currently Amended) The cache memory according to Claim 1,

wherein each cache entry has a dirty flag for each of a plurality of sub-lines making up one line, and

said write back unit ~~is operable to write back~~ writes back, to the memory, only a dirty sub-line of the cache entry selected by said selection unit.

8. (Currently Amended) A control method for use in a cache memory, comprising:

storing an address range into a specified register through execution of a data transfer instruction by a processor;

searching for a cache entry holding line data within the address range stored in the register;

~~an addition step of~~ adding, to each ~~cache entry~~ of the searched cache entries holding line data, a caching termination attribute indicating whether or not caching of the cache entry is allowed to be terminated, while the cache memory is not being accessed by the processor;

~~a selection step of~~ selecting a cache entry that has been added with a caching termination attribute indicating that caching is allowed to be terminated, and has been set with a dirty flag indicating that the cache entry has been written into; and

~~a write back step of~~ writing back, to a memory, line data of the selected cache entry,

regardless of an occurrence of a cache miss.

9. (New) The cache memory according to Claim 1,

wherein said addition unit comprises a command holding unit which holds, as a command, a cache memory operation performed by said addition unit, said command holding unit being configured of a register accessed by the processor through an instruction, and

said setting unit sets the caching termination attribute indicating that caching is allowed to be terminated, while said cache memory is not being accessed by the processor, when a command for setting the caching termination attribute is stored in said command holding unit.